TEMIC

Digital Integration

Design done by TEMIC

Introduction

When integrating the digital part of modern electronic system, various technical and financial criteria are considered.

Over 10 years of ASIC experience have shown that no methodology can meet them all in the same time. TEMIC experience at proposing its customers the most appropriate solution has become an art, resulting in long-term partnership.

Our customers/partners have themselves experienced several ways of doing ASICs, from the use of heavy internal investment with their own design centers, to the full sub-contracting to ASIC vendors from mere product specifications.

Know-how protection, engineering workload management and evolution of merchant CAD tools have been leader factors in the evolution of the preferred solutions.

The border between the own skills of equipment manufacturers and those of semiconductors makers has evolved : high level behavioral description -such as VHDL - has become the most appropriate language for users to bridge between system description and physical implementation.

On the other end, submicron electronics and faster digital systems have revealed new challenges to cope with the electrical behavior of signals, both on and outside the chip. For instance, clock or signal skews, cross-talks, noise, electromagnetic emission or susceptibility have become the main drivers of first-pass yields in design.

Testing of largely integrated systems -sometimes including processor cores- is also a matter of many trade-offs between circuit cost, development time and safety operation.

New generations of programmable devices such as CPLD or FPGA have also appeared, offering unbeatable flexibility and development time, but with many drawbacks in cost, sourcing , logistics, reliability, etc.

On top of the long experince of our designers, TEMIC has developed an unmatched choice of ASIC solutions offering the best trade-off in development or production cost, flexibility or performance.

Our solutions are also compatible with previous choices or vendor policies from our clients. On top of our proven capacity to deliver high-quality silicon devices in volume, we are recognized for helping them to find the way to secure their present or future supplies, while remaining competitive along the lifetime of their systems.

TEMIC is committed to help its clients to save time, money, while avoiding thrilling hassle.

Digital Integration

Design done by TEMIC

After agreement on the required specification between Customer and MHS, design is fully done by MHS from specification to final postlayout simulation. MHS will ask for Customer agreement on specific items or for final simulation result before wafer processing.

All BICMOS design are handled as Full Custom Designs whatever the physical implementation is.

Full Custom Designs

Description

Full Custom offering is a turnkey solution proposed by MHS to develop optimised circuits for cost sensitive, medium complexity CMOS ASICs with high production volume.

Automated Custom can mix any MHS physical implementation Arrays, Composite Arrays Cell Based and Full Custom " A LA CARTE" blocks.

MHS will use its system expertise in different applications.

For example :

– Automotive :	dash board controller
	network protocol controller
– Telecom :	PLL
	IQ Modulator
	V110, V120 protocol controller
	ATM/SDH interface up to 622 MHz
– Computer :	Tag ASICs

Using every available CMOS process MHS offers optimised solutions for digital integration.

Full Custom

BiCMOS Design

Due to the fact that high speed, is the key feature of BiCMOS process, MHS can develop on a turnkey basis BiCMOS designs using predefined Gate Arrays, or pure Full Custom Designs.

Electrical simulation are necessary. MHS will optimise speed, high sink or source current, noise immunity, packaging in compliance with customer request.

MF 0.8 µm BiCMOS Gate Array

Description

MF are high speed gate array combining 10 GHz NPN bipolar transistors, with CMOS 0.8 µm, 2 metal layer technology. Mixing bipolar and CMOS devices in unit circuits of ASICs, MHS BICMOS technology provides both speed performances, compatible with bipolar LSIs and integration close to that of CMOS LSIs, keeping low power competitiveness.

Features

- BICMOS technology – CMOS 0.8 µm, 2 metal + NPN bipolar transistor
- High level of utilisation
  –Up to 85 %
- Large range of operating modes :
  –CMOS/TTL/PSEUDO ECL (0 – +5 V)
  –ECL (–5 V – 0)
  –Mixed mode (–5 V – 0 – +5 V)
- High speed performance :
  –CMOS NAND2 typical delay : 0.44 ns (FANOUT 4- - -)
  –BICMOS NAND2 typical delay : 0.29 ns (FANOUT 4- - -)
  –TTL input buffer delay : 0.95 ns (FANOUT <= 10)
  –32 mA TTL fast output buffer : 1.3 ns
  (LOAD : R = 390 Ohm, C = 50 pF)
  –32 mA ECL output buffer : 0.75 ns (LOAD : R = 50 Ohm, C = 50 pF)
- Flexible I/O configuration : input, output, three-state, bi-directionnal, VCC, GND, VEE
- 3 output buffer options : fast, normal, low noise
- 10 K, 100 K ECL standards supported
- Programmable output drive from 3.2 to 40 mA (SINK, SOURCE), parallelism up to 64 mA
- Optional D-latch in each I/O
- Dedicated software for optimum memory integration
- Class 2 & latch-up free
- Max toggle frequency : 500 MHz

Product Outline

Type	Total Gates	Max Estimated Usable Gates**	Maximum Programmable I/O
MF5K	5220	4700	76
MF13K	13536	12100	120
MF32K	32832	26300	186
MF50K	50196	37700	232
MF92K*	92232	64500	316

* On request.
** Depending on the application.

I/O Flexibility

MHS BICMOS gate array concept can cope with CMOS/TTL requirements as well as ECL and PSEUDO-ECL interfacing.

The peripheral basic cell was built to guarantee the right POWER SUPPLY implementation next to any I/O type :

– VCC and GND, or GND and VEE for CMOS/TTL or ECL interfaces
– VCC, GND and GND, VEE in case of mixed mode (2 supplies are needed).

Inputs

Each input can be programmed as CMOS, TTL, PSEUDO-ECL, ECL classical interface. SCHMIDTT TRIGGER with or without PULL-UP/PULL-DOWN resistor are also available for CMOS/TTL applications.

Outputs

From a single output buffer, CMOS, TTL, PSEUDO-ECL drives are available.

For switching noise and power comsumption reduction, CMOS and TTL outputs, provide slew-rate and current drive adjustment facilities.

Current drive capacities are 12, 24, 32, 40 mA (64 mA available with parallelism).

SLEW RATE is controlled by different resistor values within 3 buffer types :
– Fast output buffer
– Normal output buffer
– Low noise output buffer

As a matter of fact, the intrinsec propagation delay is increased while reducing the noise.

ECL 10K and ECL 100K standards are supported by dedicated buffers. Beware of ECL 100K standard definition which doesn't obviously fit with military specifications.

Power Supply Requirements

To provide clean supplies rails to all parts of the matrix, and for a better current density control, 3 different areas are isolated :
– the CORE
– the QUIET PART of the buffers (close to the core)
– the POWER PART of the buffer (close to the pad)

Absolute Maximum Ratings

Ambient temperature under Bias (TA) :
Commercial : . . . . . 0°C to +70°C
Industrial : . . . . . –40°C to +85°C
Military : . . . . . –55°C to +125°C
Maximum Junction temperature : . . . . . 150°C
Storage temperature : . . . . . –65°C to +150°C
TTL/CMOS :
Supply voltage VCC : . . . . . –0.5 V to +7 V
I/O voltage : . . . . . –0.5 V to VCC + 0.5 V
ECL :
Supply voltage VEE : . . . . . +0.5 V to –7 V
I/O voltage : . . . . . +0.5 V to VEE – 0.5 V

Stresses at or above those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics Example (TA = 25°C)

Specified at VCC = +5V when CMOS/TTL and VEE = –5V when ECL

Symbol Type	Macro	Description	Typical Progration Delay (ns) Fanout			
			2	4	6	8
CMOS tP BICMOS tP	NAND2	2–input NAND	0.33 0.24	0.44 0.29	0.55 0.33	0.64 0.36
CMOS tP D2QWh CK	DFFR1	D Flip–Flop with positive Reset	0.89	1.10	1.27	1.45
tPLH tPHL	BUFINMOS	CMOS input Buffer	0.54 0.48	0.56 0.51	0.57 0.52	0.59 0.54
tPLH tPHL	BUFINTTL	TTL input Buffer	0.82 1.05	0.84 1.07	0.85 1.08	0.86 1.12
tPLH tPHL	BUFINECL	ECL input Buffer	0.71 0.82	0.72 0.82	0.73 0.85	0.76 0.88
ns			1 SUPPLY	2 SUPPLIES	LOAD	
tP	BU...	fast TTL buffer normal TTL buffer low noise TTL buffer	1.30 2.45 6.20	2.25 3.45 7.15	50pf, 390 OHM 50pf, 500 OHM 50pf, 500OHM	
tP	BU...	fast CMOS buffer normal CMOS buffer low noise CMOS buffer	1.50 2.60 6.35	2.35 3.65 7.35	50pf, 390 OHM 50pf, 500 OHM 50pf, 500OHM	
tP	BU...	ECL 10K buffer ECL 100K buffer	0.75 0.75	0.75 0.75	15pf, 50 OHM 15pf, 50 OHM	

MFRT : Radiation Tolerant 0.8 µm BiCMOS Gate Arrays

Description

TEMIC / MATRA MHS is the first European supplier for space application submicronic radiation tolerant gate arrays.

This is why TEMIC keeps offering a fluent way of moving up and down the quality and the space/radiation tolerant capability of its products offering, and makes available its advance submicronic BiCMOS MF gate arrays family, through a mask compatible space / radiation tolerant process, so called ”MFRT” : this is the result of the TEMIC “Dual Use Technology” strategy serving the AMS (Avionics, Military & Space) market segments.

It offers the user to either go directly to a radiation tolerant prototypes and flight models delivery, or to start with cheaper non radiation tolerant prototypes, converting, then, to a radiation tolerant version, only when EQM or FM are actually needed, provided proper simulations have been run before going either way.

Features

- mask compatible radiation tolerant version of the MF gate arrays family
- no rebound effect demonstrated after annealing
- total dose capability evaluated on a design basis
- positive influence of space very low dose rate (< 1 rad/h) expected
- latch up free : better than 100 MeV
- SEU threshold better than 50 MeV
- suitable for most space projects, LEO, GEO or POLAR orbits and deep space,
- advance very low power 0.8 µm BiCMOS process
- total dose effect simulation through Kd
- dedicated space design rules checkers

Basic Flow

The MFRT design flow follows the standard MF one, with specific space design rules which can be verified with dedicated space design rules checkers.

The simulation tools allow to verify that under any level of total dose up to 85 Krad, the functionality and the speed performances are still met.

When the ASIC to be designed is to be procured to quality grades as MIL-STD-883 class S or SCC9000 level B, then a restriction shows up because of the die size, limiting the use of matrices to the MF50KE (the E stands for the RT version), at the best.

The packages offering takes benefit of what has been set for the MCRT and is as follows :

- multi layers quad flat package with up to 256 pins, J, gull wing or flat leaded,
- side brazed technology with up to 64 pins.

So as to allow efficient design flow at both component and system levels, TEMIC has set an efficient route from the prototyping for A or B models, to flight models representative for EQM, delivering.

After negotiation, TEMIC can also offer a full service for :

- either a radiation evaluation on a batch per batch basis,
- or a radiation lot acceptance test (RLAT)

Finally, and as a natural consequence of our “dual use technology”, for the purpose of better silicon usage efficiency and better performances, our composite MFM offering is also available for space applications with the same features and capabilities as our “MFM” and “MFRT” as a full custom.

Propagation Delay Factors

Propagation delays are a function of several factors, including fanout, interconnection capacitance, supply voltage, junction temperature, and process tolerance.

To convert nominal delay values (VCC = 5 V, TA = 25°C, Typical process), into worst case ones the user has to apply derating coefficients Kp, Kv, Kt which are displayed below.

Process
$0.7 < k_p < 1.4$

Voltage	KV
4.50V	1.09
4.75V	1.04
5.00V	1.00
5.25V	0.95
5.50V	0.89

Temperature	KT
–55°C	0.80
–40°C	0.84
0°C	0.91
25°C	1.00
75°C	1.09
125°C	1.21

Packaging

MHS offers a wide rang of packaging options including CPGA, CQFP, SOIC, PLCC, CLCC, QFP, Wafer, Dio. For BiCMOS devices, packaging must be chosen according to speed and power consumption specification.

On top of that MHS offers optimal associations, package/BiCMOS MATRIX for power dissipation control and thermal management.

These associations were checked by thermal simulations, taking care of the maximum accepted junction temperature, and the context of the application (temperature, air speed, thermal exchanges etc.)

Type	MF5K	MF10K	MF32K	MF54K	MF92K	Pins
Copper lead frame PQFP	100	128	160	240	304 on request	”
MQUAD (R)	_	128	208	240	on request	”
Heat sink MQUAD (R) down		128 *	208 *	240 *	on request	”
Alumina cerquad	100	132 / JEDEC 128 / EIAJ	196 / JEDEC *	240	304 on request	” ”
Multilayer Alumina quad pack	CLCC 84	132 / JEDEC	196 / JEDEC	256 / JEDEC	348 / JEDEC	”
Heat sink multilayer Alumina quad pack	_	on request	on request	on request	on request	”
Alumina PGA	100	144	209	299	340 D	”
Heat sink Alumina PGA	on request	144 D	207 D *	300 D	340 D	”

(R) Registered Product of olin
* Special pattern

It is mandatory before final package selection, to compute power consumption calculation, and check with MHS offices, the right package solution.

MFM : 0.8µm BiCMOS Composite Gate Arrays

Description

TEMIC/ MATRA MHS, taking advantage of being also a standard ICs manufacturer (SRAM, DPRs, FIFOs,...) bridges the gap between full custom designs and gate arrays with its so called “Composite” concept, offering the possibility to merge hard blocks into arrays of standard spare gates, so as to get :

- faster speed,
- lower power consumption,
- higher density, preventing from design partitioning,

offering the best trade off between low design cost and short prototyping cycle time, and high integration density.

Features

- advance very low power 0.8 µm BiCMOS process
- allows high level of local integration and high speed performances with :
  - mega blocks from customers or TEMIC libraries
  - COMPASS compiled blocks (two port RAM, data path,...)
  - TECHGEN for RAM and ROM generation

Basic Flow

The MFM design flow follows the standard MF ones, but as a full custom service, once one has defined the blocks and the number of spare gates with their floor plan, the user operates as with a standard gate array. If the content of the array has been agreed before the design is completed and signed off, TEMIC manages to process the first steps of the silicon process, allowing to start immediately the metallization layers once design signed off.

The package styles offering is similar to MF offering.

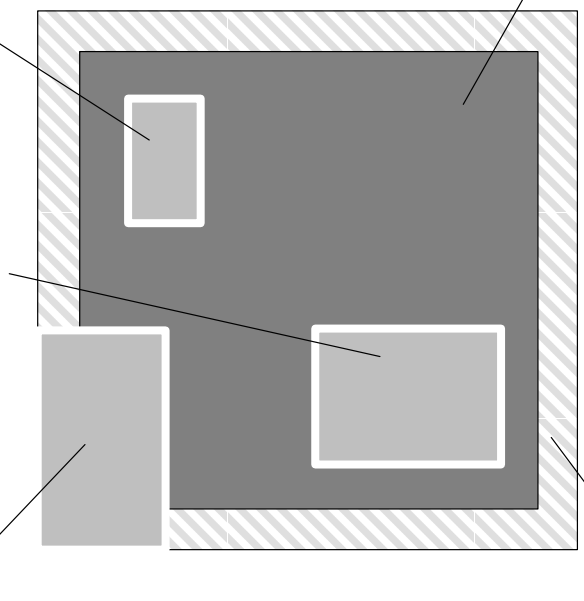
Finally, and as a natural consequence of TEMIC “dual use technology”, the composite MFM offering is also available for space applications with the same features and capabilities as our “MFM” and “MFRT”, but as a full custom service.

Full Custom

Composite Array : BiCMOS 0.8µm

- **Hard cells**
  - RAM/ROM/FIFO
  - Multiplier, Adder
  - Multiport RAM
  - Imported GDSII blocks

- **Application specific cells**
  - ABUS, VAN, CAN*
  - CAM, Smart RAMs
  - AAL*, CRC*



- **Cells : Optimised for Automatic syntheses**
- **Macrocells**
  - Coder, decoder
  - Arithmetic function
  - Counter, register...
- **MEGA Cells**
  - Microcontroller peripherals (8251, 59, ...)
  - Protocol controllers (X21, I2C, V110, V120, ...)
  - UART
- **Gate based RAM generator**
- **Synthetised blocks**

- **Interface blocks**
  - A/D, D/A
  - ATM 155/622 Mbit/s

- **Peripheral pads**
  - TTL/CMOS/ECL
  - Pseudo ECL/BTL

* under development

Design Flows

Design Offering

Five different ASIC design offerings are available : ULC, Gate Arrays, Composite Arrays, Cell Based and Full Custom, each physical implementation giving an answer to the compromise : flexibility/unit price and integration/development cost.

Design Modes

Three different design modes can be agreed between Customer and MHS, depending on system and integration skills requirements.

Mode	Logic Design	Physical Layout	Design Tools
Customer Design	Customer	Customer	Customer tools
Customer and TEMIC Design	Customer	MHS	MHS supported tools (Netlist and simulation)
TEMIC Design	MHS	MHS	MHS supported tools (Netlist and simulation)

Supported tools are currently CADENCE, COMPASS, MENTOR, SYNOPSYS and VHDL/VITAL.

Design Modes versus Design Offering

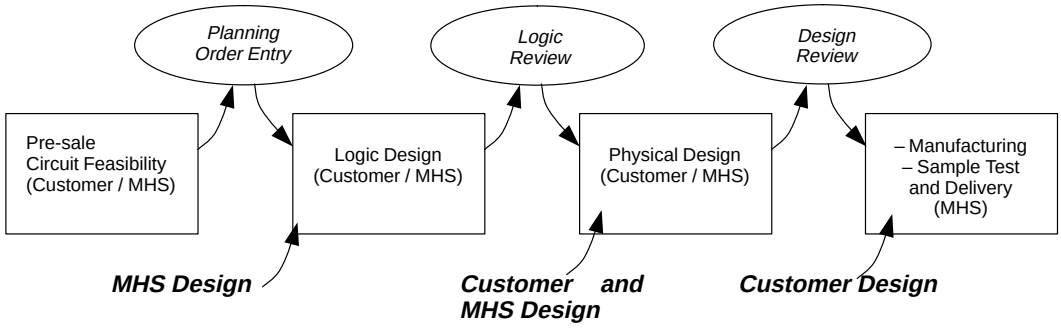
Offering \ Mode	Customer Design	Customer and MHS Design	MHS Design
ULC			□
Gate Array		x	□
Composite Array		x	□
Cell Based	x	○	□
Full Custom	x		

x : standard offer.
○ : depending on human and hardware ressources needed and/or available.
□ : specific development using MHS own expertise.

Design Phases and Meetings

The design of a circuit is separated into four main phases, separated by three major meetings between MHS and the Customer, as shown in Figure 1.

Figure 1. The design phases and meetings.



Digital Integration

Processes

Description

MHS develops a wide range of CMOS processes, used for catalog products or ASICs' volume production. Their common features are high performance / high speed both with low power consumption, either in stand–by or operating modes.

MHS/TEMIC makes those processes available for selected customers/partners for their own design.

Features

	Technology	Well	Lithography (µm)	Poly Layers	Metal Layers	Operating Voltage (VO)	Characteristics
Digital Series							
FCC1D	CMOS	N	0.8	1	2	5 or 3	
FCC1S	CMOS	N	0.8	1	1	5 or 3	
FCC2D	CMOS	Twin	0.6	1	2	5 and/or 3	
FCC2T	CMOS	Twin	0.6	1	3	5 and/or 3	
FCB1D	BICMOS	Twin	0.8	1	2	5 and/or 3	NPN
Mixed Analog / Digital Series							
FCA1D FCA2D (1) FCA2T (2)	CMOS CMOS CMOS	N N	0.8 0.6 0.6	2 2 2	2 2 3	5 and/or 3 5 and/or 3 5 and/or 3	Low V_t
Non Volatile Series							
FCN1D FCN2D (1) FCN2T (2)	CMOS CMOS CMOS	2 2 2	0.8 0.6 0.6	1 1 1	2 2 3	5 5 and/or 3 5 and/or 3	EPROM EPROM
Radiation Tolerant Series							
FCT1D FCBTD FCT2D	CMOS BICMOS CMOS	N Twin Twin	0.8 0.8 0.6	1 1 1	2 2 3	5 5 5 and/or 3	Guard Ring Guard Ring Guard Ring

(1) Under Development (2) Planned

MHS Processes include digital CMOS processes and several derivatives done from the CMOS core basis :

- mixed analog/digital series with one more polysilicon layer and low V_t transistors
- non volatile series with high voltage NMOS transistors and programming/sensing/erasing capabilities
- radiation tolerant process with specific guard rings